CLAIMS

Claims 39, 41 and 44-52 are cancelled.

53. (New) A semiconductor processing method of depositing SiO_2 on a substrate comprising:

providing a substrate within a chemical vapor deposition reactor;

forming a liquid mixture comprising an organic silicon precursor and at least one of H_2O and H_2O_2;

converting the liquid mixture into a gaseous mixture;

feeding the gaseous mixture into the chemical vapor deposition reactor; and

utilizing the gaseous mixture, depositing a layer of SiO_2 on the substrate at a rate of about 7000 Å per minute

F1

54. (New) The semiconductor processing method of claim 53 wherein the liquid mixture comprises no less than about 0.5% by volume of the at least one of H_2O and H_2O_2.

55. (New) The semiconductor processing method of claim 53 wherein the liquid mixture comprises from about 5% to about 15% by volume of the at least one of H_2O and H_2O_2.

G

56. (New) The semiconductor processing method of claim 53 wherein the converting comprises heating the liquid to a temperature of from about 65°C to about 80°C.

57. (New) The semiconductor processing method of claim 53 wherein the chemical vapor deposition reactor is a cold wall, low pressure chemical vapor deposition reactor.

58. (New) The semiconductor processing method of claim 53 wherein the silicon precursor is selected from the group consisting of: tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclo-tetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).

59. (New) The semiconductor processing method of claim 53 wherein during the depositing the reactor comprises an internal pressure of from about 10 Torr to about 80 Torr.

60. (New) A semiconductor processing method of depositing SiO_2 on a substrate comprising:

providing a substrate within a chemical vapor deposition reactor;

feeding a gaseous silicon precursor into the chemical vapor deposition reactor;

feeding gaseous H_2O_2 into the chemical vapor deposition reactor; and

utilizing the silicon precursor, depositing a layer of SiO_2 over a surface of the substrate at a rate of about 7000 Å per minute.

61. (New) The semiconductor processing method of claim 60 wherein the gaseous H_2O_2 and the gaseous silicon precursor are fed into the chemical vapor deposition reactor independently.

62. (New) The semiconductor processing method of claim 60 wherein the gaseous H_2O_2 and the gaseous silicon precursor are fed into the chemical vapor deposition reactor simultaneously.

63. (New) The semiconductor processing method of claim 60 wherein the gaseous H_2O_2 and the gaseous silicon precursor are combined prior to feeding into the chemical vapor deposition reactor.

64. (New) The semiconductor processing method of claim 60 further comprising feeding gaseous H_2O into the chemical vapor deposition reactor.

65. (New) The semiconductor processing method of claim 60 wherein the providing a substrate within a chemical vapor deposition reactor comprises providing a wafer gap to susceptor distance of about 230 mils.

66. (New) The semiconductor processing method of claim 60 wherein the surface of the substrate comprises a high aspect ratio topology and wherein the layer is conformally deposited over the topology.

67 (New) The semiconductor processing method of claim 60, wherein the silicon precursor is selected from the group consisting of: tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclo-tetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).